REMARKS

In view of the following remarks, Applicants respectfully request reconsideration and allowance of the subject application. This amendment is believed to be fully responsive to all issues raised in the Office Action mailed January 9, 2004.

Claim Rejections

Rejections Under 35 U.S.C. §112

Claim 8 was rejected under 35 U.S.C. §112, second paragraph. Claim 8 has been amended to address the rejection.

Rejections Under 35 U.S.C. §102

Claims 1-4, 7-13, and 15-17 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,790,782 to Martinez, et al. (hereinafter, "the '782 patent"). Applicants traverse the rejections of claims 1-4 and 7-9. Anticipation under 35 U.S.C. §102 requires that *each and every element* of the claim be set forth in the manner recited in the claim in a single prior art reference. (See, MPEP 2131). The '782 patent fails to disclose at least one limitation of independent claim 1. Therefore, the 782 patent cannot anticipate independent claim 1.

Independent claim 1 positively recites "a first junction box . . . for providing a first shelf identifier signal to a device enclosure connected to the first shelf; and a second junction box linked to the first junction box . . . for providing a second shelf identifier signal to a device enclosure connected to the second shelf." The Action asserts that the '782 patent discloses this

limitation, and cites Fig. 1, elements 15, 16, 17 and column 4, lines 8-33 to support the rejection. Applicants disagree. The cited text reads as follows:

> FIG. 1 provides a front view of a vertically extending cabinet 10 having four shelves, i.e. shelf-1 identified by numeral 11, shelf-2 identified by numeral 12, shelf-3 identified by numeral 13, and shelf-4 identified by numeral 14. Note that in this nonlimiting example, the shelves are configured in a top-to-bottom physical/logical sequence configuration.
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> By way of dotted lines, FIG. 1 illustrates that cabinet 10 may include the number "M" of individual shelves, in which case a 3-shelf group "N-1", "N" and "N+1" is also provided.
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> Each shelf within cabinet 10 is provided with a pair of lower-disposed and redundant input-ports or connectors 15, and a pair of upper-disposed and redundant output ports or connectors 16. Note that the two upper output ports 16 of a lower shelf, for example shelf-2, are located closely adjacent to the two lower input ports 15 of the next adjacent shelf-3. As will be appreciated, ports 15 can also be called receiver ports, whereupon ports 16 would be called transmitter ports.
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> In accordance with a feature of this invention, the adjacent shelf ports 15,16 are connected by way of a short-length, 2-wire, cable 17 that prevents an inadvertent misconnection between the output port of a lower shelf and a port of another shelf. By way of example, cables 17 are about 6 inches long.
>
> As seen in FIG. 1, the top shelf, be it shelf-4 or shelf-M, does not have a cable 17 connected to its top disposed redundant pair of output ports 1.

Nothing in this text discloses (or even suggests) structure corresponding to the first and second junction boxes, as explicitly recited in claim 1. The elements 15 and 16 are identified as shelf ports. The element 17 is identified as a cable. The '782 fails to disclose structure corresponding to junction boxes. Therefore, the '782 patent cannot anticipate independent claim 1.

Applicants note that claims 2-4 and 7-9 depend from independent claim 1, and are allowable by virtue of their dependency. In addition, dependent claims recite features neither disclosed nor suggested by the'782 patent.

By way of example, dependent claim 2 recites the limitation that "the first and second junction boxes each include an additional output connection at third and fourth shelves of the cabinet for providing third and fourth shelf identifier signals differing from the first and second shelf identifier signals, respectively." The Action asserts that the '782 patent discloses this limitation, and cites Fig. 1, elements 11, 16, 15 and 12-14, and column 2, lines 33-44 and column 5, lines 39-57 to support the rejection. Applicants disagree. The cited text reads as follows:

> A true shelf physical location to shelf logical or data processing address is achieved because;
> (1) an individual inter shelf cable is used only to attach two adjacent shelves,
> (2) the shelves are physically mounted into the cabinet in a physical sequence, for example, from the bottom up, from the top down, from right to left, or from left to right, and
> (3) shelf logical or data processing addresses are assigned to the shelves in this same sequential order, i.e. from the bottom up, from the top down, from right to left, or from left to right.
>
> In FIG. 6, the input connector 16 and the output connector 15 of shelf "N" are shown connected to the next lower shelf "N-1" and to the next higher shelf "N+1" by way of two short-length cables 17, as was above described relative to FIG. 1.
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> In accordance with this invention, input connector 16 of shelf "N" is provided with an analog voltage 35 whose analog magnitude comprises the decimal equivalent of the following binary value;—(the binary address of shelf "N"-1) plus (a binary one). For example, assume that the shelf address of shelf "N-1" is decimal-5. The

> 5-bit binary address of shelf "N-1" is therefor "00101". As a result, shelf "N-1" provides and output voltage 35 to shelf "N" having an magnitude that is the equivalent of binary "00110". As will be apparent from the following description, the EMU 21 that is within shelf "N-1" has operated to ensure the magnitude of analog voltage 35 comprises the correct address for shelf "N".

Nothing in this text discloses (or even suggests) structure corresponding to the first and second junction boxes, much less to first and second junction boxes which each include an additional output connection at third and fourth shelves of the cabinet for providing third and fourth shelf identifier signals differing from the first and second shelf identifier signals, respectively, as explicitly recited in claim 2. Therefore, the '782 patent cannot anticipate independent claim 2.

Dependent claim 3 recites the limitation that "each of the junction boxes includes a sensing wire providing signals to the output connections and being alternately grounded and open to differentiate the first and second shelf identifier signals from the third and fourth shelf identifier signals." The Action asserts that the '782 patent discloses this limitation, and cites Fig. 6, elements 43 and 35 to support the rejection. Applicants disagree. Elements 43 and 35 of Fig. 6 are identified as an analog next-shelf-address signal and an analog shelf address signal, respectively. Nothing in Fig. 6 or the accompanying text discloses a sensing wire that is alternately grounded and open to differentiate the first and second shelf identifier signals from the third and fourth shelf identifier signals, as recited in claim 3. Therefore, the '782 patent cannot anticipate claim 3.

Dependent claim 7 recites the limitation that "the sensing wires of the first and second sets are passed through the first junction box and are

included in the output signal to the second junction box and further wherein each of the sensing wires in the first set are moved one position within the first set and each of the sensing wires in the second set are moved one position within the second set prior to the link with the second junction box."

The Action asserts that the '782 patent discloses this limitation, and cites column 5, lines 39-67 and column 6, lines 1-34 to support the rejection. Applicants disagree. The cited text reads as follows:

> In FIG. 6, the input connector 16 and the output connector 15 of shelf "N" are shown connected to the next lower shelf "N-1" and to the next higher shelf "N+1" by way of two short-length cables 17, as was above described relative to FIG. 1.
>
> In accordance with this invention, input connector 16 of shelf "N" is provided with an analog voltage 35 whose analog magnitude comprises the decimal equivalent of the following binary value;--(the binary address of shelf "N"-1) plus (a binary one). For example, assume that the shelf address of shelf "N-1" is decimal-5. The 5-bit binary address of shelf "N-1" is therefor "00101". As a result, shelf "N-1" provides and output voltage 35 to shelf "N" having an magnitude that is the equivalent of binary "00110". As will be apparent from the following description, the EMU 21 that is within shelf "N-1" has operated to ensure the magnitude of analog voltage 35 comprises the correct address for shelf "N".
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> The 5-bit binary number now stored in register 38 is now presented to a network 39 that operates to increment the binary stored content of register 38 by a binary-1. As a result, the data processing address of shelf "N" has been incremented by "1", and in this manner, the data processing address of shelf "N+1" has been generated on conductor 40. This next-shelf-address 40 is now stored in 5-bit output register 41 and is presented to bus or cable 44.
>
> A Digital to Analog Converter (DAC) 42 now operates to convert this next-shelf-address 44 into an analog voltage 43 whose magnitude is representative of the magnitude of the binary number that comprises next-shelf-address 44.

> This analog next-shelf voltage 43 is now presented to input connector 16 of shelf "N+1".
>
> In order to ensure that analog voltage 43 is of the correct "next shelf address" magnitude, and to thereby provide a correct binary data processing address for next shelf "N+1", analog voltage 43 is now presented as an input to ADC 45. The binary output 46 of ADC 45 is then stored in 5-bit output compare register 47. The stored content of register 47 should be the data processing address of next shelf "N+1".
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> In order to effect this error detection, a digital output compare network 48 it provided with a first input that comprises the 5-bit output 49 of compare register 47 and a second input that comprises the 5-bit output 44 of output register 41. So long as these two 5-bit binary values are of the same magnitude, no error signal 50 is reported to server 30 of FIG. 5 by way of bus 32. However, when the two binary values 44,49 are not of the same magnitude, this lack of compare is taken as a detection of the fact that the EMU 21 of shelf "N" has failed to generate the proper next-shelf-address for application to the input connector 16 of shelf "N+1".
>
> While the above description has dealt with the use of 5-bit registers, it will be recognized that this detail of description is not to be taken as a limitation on the invention.

Nothing in this text discloses (or even suggests) structure corresponding to the first and second junction boxes or sensing wires within the junction boxes much less an arrangement in which each of the sensing wires in the first set are moved one position within the first set and each of the sensing wires in the second set are moved one position within the second set prior to the link with the second junction box, as explicitly recited in claim 7. Therefore, the '782 patent cannot anticipate independent claim 7.

Independent claim 10 has been amended to positively recite the limitation that the cabinet bus is adapted to generate and to provide a unique shelf identifier to each of the shelves. This limitation is neither disclosed nor suggested by the '782 patent. To the contrary, the cable 17 disclosed in the

'782 patent is entirely passive. Identification signals are generated by the circuitry of Fig. 6. Accordingly, claim 10 is allowable over the '782 patent.

Claims 11-18 depend ultimately from claim 10, and are allowable at least by virtue of this dependency. In addition, claims 11-18 recite specific structural limitations neither disclosed nor suggested by the '782 patent.

Rejections Under 35 U.S.C. §103

Claims 19 was rejected under 35 U.S.C. §103(a) as being unpatentable over the '782 patent in view of the '782 patent"). Independent claim 19 has been amended to positively recite the limitation that the cabinet bus is adapted to generate and to provide a unique shelf identifier to each of the shelves. This limitation is neither disclosed nor suggested by the '782 patent. To the contrary, the cable 17 disclosed in the '782 patent is entirely passive. Identification signals are generated by the circuitry of Fig. 6. Accordingly, claim 19 is allowable over the '782 patent.

Claims 20-21 depend ultimately from claim 19, and are allowable at least by virtue of this dependency. In addition, claims 20-21 recite specific structural limitations neither disclosed nor suggested by the '782 patent.

CONCLUSION

Claims 1-21 are believed to be in condition for allowance. Applicants respectfully request reconsideration and prompt issuance of the present application. Should any issue remain that prevents immediate issuance of the application, the Examiner is encouraged to contact the undersigned attorney to discuss the unresolved issue.

Respectfully Submitted,
Jed W. Caven
Attorney for Applicants

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Jed W. Caven
Lee & Hayes, LLP
Reg. No. 40,551
(303) 539-0265 x 246

Direct correspondence to:
Hewlett-Packard Company
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400